CLAIMS

We claim:

1. An apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer, the apparatus comprising:

a receptacle having a plurality of section walls;

a wafer chuck configured to hold the semiconductor wafer and to position the semiconductor wafer within the receptacle with a surface of the semiconductor wafer adjacent to top portions of the plurality of section walls; and

a first plurality of sensors configured to measure alignment between a center of one of the plurality of section walls to a center of the wafer chuck.

2. The apparatus of claim 1, wherein the center of the one of the plurality of section walls is aligned with a center of the semiconductor wafer within a tolerance in a range of 0.001 mm to 1 mm.

3. The apparatus of claim 2, wherein the tolerance is less than 0.01 mm.

4. The apparatus of claim 2, wherein the plurality of section walls are cylindrical and concentric.

5. The apparatus of claim 1, wherein the first plurality of sensors includes a first sensor pair comprising:

a first sensor disposed on one of the plurality of section walls; and

a second sensor disposed on a circumference of the wafer chuck.

6. The apparatus of claim 5, wherein the first sensor is embedded in one of the plurality of section walls.

7. The apparatus of claim 1, wherein the first plurality of sensors includes a first sensor pair comprising:

a first sensor disposed on a perimeter wall of the receptacle; and

a second sensor disposed on a circumference of the wafer chuck.

8. The apparatus of claim 7, wherein the first sensor is embedded in the perimeter wall.

9. The apparatus of claim 8, wherein the first sensor is a sensor ring formed on a top portion of the perimeter wall.

10. The apparatus of claim 7, wherein the second sensor is embedded in the wafer chuck.

11. The apparatus of claim 1, wherein the first plurality of sensors includes:

a first sensor pair configured to provide a first measurement of a gap between the wafer chuck and one of the plurality of section walls; and

a second sensor pair configured to provide a second measurement of a gap between the wafer chuck and one of the plurality of section walls.

12. The apparatus of claim 1, wherein the first plurality of sensors includes:

a first sensor pair configured to provide a first measurement of a gap between the wafer chuck and a perimeter wall of the receptacle; and

a second sensor pair configured to provide a second measurement of a gap between the wafer chuck and the perimeter wall of the receptacle.

13. The apparatus of claim 1, wherein the first plurality of sensors includes:

four sensors equally distributed in a circumference of the top portion of one of the plurality of section walls; and

four sensors equally distributed in a circumference of the wafer chuck.

14. The apparatus of claim 1, wherein the first plurality of sensors includes optical reflectivity sensors, magnetic sensors, capacitance sensors, or ultrasonic sensors.

15. The apparatus of claim 1, further comprising:

a second plurality of sensors configured to measure a gap between the semiconductor wafer and the top portions of the plurality of section walls.

16. The apparatus of claim 15, wherein the gap between the semiconductor wafer and the top portion of the plurality of section walls is between a range of 0.5 millimeters to 10 millimeters.

17. The apparatus of claim 16, wherein the gap is 5 millimeters.

18. The apparatus of claim 15, wherein the second plurality of sensors includes:
a first sensor disposed inside a bottom of the receptacle; and
a second sensor disposed on the wafer chuck.

19. The apparatus of claim 15, wherein the second plurality of sensors includes optical reflectivity sensors, magnetic sensors, capacitance sensors, or ultrasonic sensors.

20. An apparatus for electropolishing and/or electroplating metal layers on a semiconductor wafer, the apparatus comprising:
a receptacle divided into a plurality of concentric sections with a center;
a wafer chuck configured to hold the semiconductor wafer and to position the semiconductor wafer within the receptacle; and
a first plurality of sensors configured to measure alignment between the center of the concentric sections and a center of the semiconductor wafer.

21. The apparatus of claim 20, wherein the concentric sections are formed by a plurality of cylindrical and concentric section walls, and wherein a surface of the semiconductor wafer to be electropolished or electroplated is positioned adjacent to top portions of the plurality of section walls.

22. The apparatus of claim 21, wherein the first plurality of sensors includes a first sensor pair comprising:
a first sensor disposed on one of the plurality of section walls; and
a second sensor disposed on a circumference of the wafer chuck.

23. The apparatus of claim 21, wherein the first plurality of sensors includes:

a first sensor pair configured to provide a first measurement of a gap between the wafer chuck and one of the plurality of section walls; and

a second sensor pair configured to provide a second measurement of a gap between the wafer chuck and one of the plurality of section walls.

24. The apparatus of claim 21, further comprising:

a second plurality of sensors configured to measure a gap between the semiconductor wafer and the top portions of the plurality of section walls.

25. The apparatus of claim 24, wherein the second plurality of sensors includes:

a first sensor disposed inside a bottom of the receptacle; and

a second sensor disposed on the wafer chuck.

26. The apparatus of claim 20, wherein the first plurality of sensors includes a first sensor pair comprising:

a first sensor disposed on a perimeter wall of the receptacle; and

a second sensor disposed on a circumference of the wafer chuck.

27. The apparatus of claim 20, wherein the first plurality of sensors includes:

a first sensor pair configured to provide a first measurement of a gap between the wafer chuck and a perimeter wall of the receptacle; and

a second sensor pair configured to provide a second measurement of a gap between the wafer chuck and the perimeter wall of the receptacle.

28. A method of electroplishing and/or electroplating metal layers on a semiconductor wafer, the method comprising:

positioning a wafer chuck holding a semiconductor wafer within a receptacle having a plurality of section walls, wherein a surface of the semiconductor wafer to be electroplished or electroplated is positioned adjacent to top portions of the plurality of section walls; and

measuring alignment between a center of one of the plurality of section walls to a center of the wafer chuck using a first plurality of sensors.

29. The method of claim 28, wherein the first plurality of sensors includes a first sensor pair and a second sensor pair, and wherein measuring alignment comprises:

measuring a first gap between the wafer chuck and one of the plurality of section walls using the first sensor pair;

measuring a second gap between the wafer chuck and one of the plurality of section walls using the second sensor pair; and

determining alignment of the wafer chuck and one of the plurality of section walls based on the measurement of the first gap and second gap.

30. The method of claim 29, wherein the first sensor pair includes:

a first sensor disposed on one of the plurality of section walls; and

a second sensor disposed on a circumference of the wafer chuck.

31. The method of claim 28, wherein the first plurality of sensors includes a first sensor pair and a second sensor pair, wherein measuring alignment comprises:

measuring a first gap between the wafer chuck and a perimeter wall of the receptacle using the first sensor pair;

measuring a second gap between the wafer chuck and the perimeter wall using the second sensor pair; and

determining alignment of the wafer chuck and the perimeter wall based on the measurement of the first gap and second gap.

32. The method of claim 31, wherein the first sensor pair includes:

a first sensor disposed on the perimeter wall; and

a second sensor disposed on a circumference of the wafer chuck.

33. The method of claim 28, further comprising:

measuring a gap between the surface of the semiconductor wafer and the top portions of the plurality of section walls using a second plurality of sensors.